Claims

1. A wafer, comprising:

an array of chips having contacts, said contacts comprising solder bumps, said array of chips including perimeter chips extending along a periphery of the wafer; and

additional dummy solder bumps located adjacent most of said perimeter chips wherein said additional dummy solder bumps are for improving contact processing of said perimeter chips.

2. The wafer as recited in claim 1, wherein said additional dummy solder bumps are for providing support for a shadow mask used to deposit a material on said solder bumps so said shadow mask does not damage perimeter chip solder bumps.

3. The wafer as recited in claim 2, wherein said solder bumps comprise a layer of said material.

4. The wafer as recited in claim 3, wherein said material comprises tin.

5. The wafer as recited in claim 3, wherein said material is deposited on reflowed bumps.

6. The wafer as recited in claim 1, wherein said additional dummy solder bumps are omitted in saw blade lanes.

7. The wafer as recited in claim 6, wherein said additional dummy solder bumps are omitted in a ring shaped exclusion region along said periphery of the wafer.

8. The wafer as recited in claim 7, wherein said additional dummy solder bumps are omitted in regions of alignment aids.

9. The wafer as recited in claim 8, wherein said alignment aids comprise a pattern of solder bumps.

10. The wafer as recited in claim 9, wherein said pattern of solder bumps comprises a pattern having a closer spacing of solder bumps than is used for contacts.

11. The wafer as recited in claim 7, wherein said additional dummy solder bumps adjacent a perimeter chip are arranged in a regular array of bumps with all positions of said array outside said saw blade lanes and said exclusion zone filled.

12. The wafer as recited in claim 1, wherein said additional dummy solder bumps comprise a single row of bumps adjacent said perimeter chips.

13. The wafer as recited in claim 1, wherein said additional dummy solder bumps comprise additional patterns of bumps corresponding to partial chips.

14. The wafer as recited in claim 1, wherein said improving contact processing of said perimeter chips is more uniform plasma etching of insulator in contacts on the wafer and lower contact resistance for perimeter chips.

15. The wafer as recited in claim 1, wherein contacts of said perimeter chips have contact resistance about equal to that of non-perimeter chips.

16. The wafer as recited in claim 1, wherein contacts of said perimeter chips have insulator about equal to that of non-perimeter chips.

17. A shadow mask, comprising:

an array of holes in the shadow mask corresponding to contacts on an array of chips on a wafer, said array of chips including perimeter chips extending along a periphery of the wafer; and

additional dummy holes in the shadow mask located adjacent holes corresponding to most of said perimeter chips wherein said additional dummy holes are for improving contact processing of said perimeter chips.

18. The shadow mask as recited in claim 17, wherein said additional dummy holes are for providing additional dummy solder bumps to support a second shadow mask used to deposit an additional layer of material on said solder bumps so said second shadow mask does not damage perimeter chip solder bumps.

19. The shadow mask as recited in claim 18, wherein said holes for depositing said additional layer of material are located in positions to compensate for the temperature of depositing tin.

20. The shadow mask as recited in claim 18, wherein said additional layer of material is for depositing through said second shadow mask onto reflowed solder bumps on chips.

21. The shadow mask as recited in claim 17, wherein said additional dummy holes are omitted in saw blade lanes.

22. The shadow mask as recited in claim 21, wherein said additional dummy holes are omitted in a ring shaped exclusion zone along said periphery of the shadow mask beyond said perimeter chips and beyond said dummy holes.

23. The shadow mask as recited in claim 17, wherein said improved contact processing of said perimeter chips is improved removal of insulator in contacts of said perimeter chips and lower contact resistance for said perimeter chips.

24. The shadow mask as recited in claim 17, wherein said additional dummy holes are located adjacent holes for substantially all of said perimeter chips.

25. The shadow mask as recited in claim 17, wherein said holes corresponding to said perimeter chips are located to compensate for the temperature of depositing chrome, copper, or gold.

26. A method of fabricating a semiconductor wafer, comprising the steps of:

(a) providing a wafer comprising an array of chips having contacts, said contacts comprising solder bumps, said array of chips including perimeter chips extending along a periphery of the wafer; and

(b) providing additional dummy solder bumps located adjacent most of said perimeter chips wherein said additional dummy solder bumps are for improving contact processing of said perimeter chips.

27. A method of fabricating a semiconductor wafer as recited in claim 26, wherein said step (b) comprises the steps of:

1. providing a wafer comprising contacts;

2. providing a shadow mask comprising additional holes corresponding to said additional dummy solder bumps, and aligning holes of said mask with contacts of said wafer;

3. plasma etching oxide in said contacts through said holes in said mask, wherein oxide in contacts of perimeter chips is etched about as well as contacts of non-perimeter chips as a result of the presence of said additional holes; and

4. depositing ball limited metallurgy and solder for solder bumps in said holes.

28. The method of fabricating a semiconductor wafer as recited in claim 27, wherein said improved contact processing of said perimeter chips is more uniform plasma etching of oxide in contacts on the wafer and lower contact resistance for perimeter chips.

29. The method of fabricating a semiconductor wafer as recited in claim 28, wherein contacts of said perimeter chips have contact resistance about equal to that of non-perimeter chips.

30. The method of fabricating a semiconductor wafer as recited in claim 28, wherein contacts of said perimeter chips have oxide about equal to that of non-perimeter chips.

31. The method of fabricating a semiconductor wafer as recited in claim 27, further comprising the step of reflowing said solder bumps.

32. The method of fabricating a semiconductor wafer as recited in claim 31, further comprising providing a solder bump cap shadow mask, wherein said step (b) of providing additional dummy solder bumps is for providing support for said solder bump cap shadow mask used to deposit a material on said solder bumps so said solder bump cap shadow mask does not damage perimeter chip solder bumps.

33. The method of fabricating a semiconductor wafer as recited in claim 32, further comprising depositing a layer of said material on said solder bumps through said solder bump cap shadow mask.

34. The method of fabricating a semiconductor wafer as recited in claim 33, wherein said material comprises tin.

35. The method of fabricating a semiconductor wafer as recited in claim 26, wherein said additional dummy solder bumps are omitted in saw blade lanes.

36. The method of fabricating a semiconductor wafer as recited in claim 26, wherein said additional dummy solder bumps are omitted in a ring shaped exclusion zone along said periphery of the wafer.

37. The method of fabricating a semiconductor wafer as recited in claim 26, wherein said additional dummy holes are located adjacent holes for substantially all of said perimeter chips.

38. A method of fabricating a shadow mask, comprising the steps of:

a) providing an array of holes in the shadow mask corresponding to contacts on an array of chips on a wafer, said array of chips including perimeter chips extending along a periphery of the wafer; and

b) providing additional dummy holes in the shadow mask located adjacent holes corresponding to most of said perimeter chips wherein said additional dummy holes are for improving contact processing of said perimeter chips.

39. The method of fabricating a shadow mask as recited in claim 38, wherein said improved contact processing of said perimeter chips is additional dummy solder bumps to support a second shadow mask used to deposit an additional layer of material on said solder bumps so said second shadow mask does not damage perimeter chip solder bumps.

40. The method of fabricating a shadow mask as recited in claim 38, wherein said additional dummy holes are omitted in saw blade lanes.

41. The method of fabricating a shadow mask as recited in claim 40, wherein said additional dummy holes are omitted in a ring shaped exclusion zone along said periphery of the shadow mask beyond said perimeter chips and beyond said dummy holes.

42. The method of fabricating a shadow mask as recited in claim 40, further comprising the step of inspecting the mask using dummy holes along an edge of a dicing lane to align the shadow mask to an inspection device.

43. The method of fabricating a shadow mask as recited in claim 40, further comprising the step of inspecting the mask using a pattern of additional holes, said additional holes located beyond holes corresponding to said perimeter chips, said additional holes for aligning the shadow mask to an inspection device, wherein said pattern of additional holes does not print on the wafer.

44. The method of fabricating a shadow mask as recited in claim 43, wherein said pattern of additional holes is located so that it will be covered by a guard ring.

45. The method of fabricating a shadow mask as recited in claim 40, further comprising the step of inspecting the mask using a covering for said additional dummy holes.

46. The method of fabricating a shadow mask as recited in claim 40, wherein said covering for said additional dummy holes is a ring having an inside edge corresponding to outside edges of perimeter chips.

47. The method of fabricating a shadow mask as recited in claim 38, wherein said improved contact processing of said perimeter chips is more uniform plasma etching of contacts on the wafer and lower contact resistance for perimeter chips.

48. A wafer, comprising:

an array of chips having solder bump contacts; and

a pattern of solder bumps for aligning the wafer with a solder bump deposition mask, the pattern of solder bumps comprising bumps having dimensions about equal to or smaller than said solder bump contacts.

49. The wafer as recited in claim 48, wherein said aligning solder bumps has a closer spacing than do said solder bump contacts.

50. The wafer as recited in claim 48, wherein said aligning solder bumps are located so as to correspond to edges of a second alignment pattern on the wafer.